ECG Simulator

Laboratory Activities
Instructor's Guide
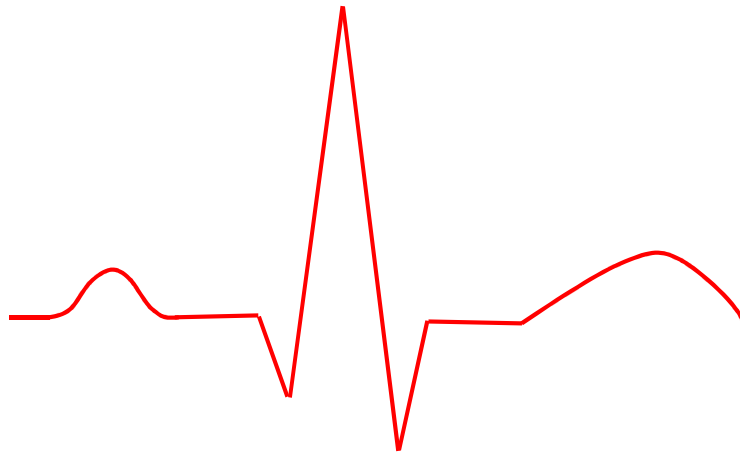
Contents

Objective

Electrocardiography (ECG) is a standard non-invasive technique for diagnostic and research of human hearts. It records the cardiac electrical waveform over a period of time. The performance of ECG monitors can be affected by many factors, such as electromagnetic noise, power fluctuations, lack of circuit grounding, measurement cables contact, electrodes attachment and circuit failures.[1] The easiest way to check whether this equipment is working properly is through an Electrocardiogram Simulator. The Engineering World Health (EWH) ECG Simulator kit is able to generate Einthoven's triangle signals (see Appendix 1 and 2) through contacts that correspond to the Left Arm (LA), Right Arm (RA) and Left Leg (LL).

The purpose of this activity is to teach engineering students the characteristics of an ECG signal and to explain the basic principles of analog and digital electronic circuits. The laboratory addresses theoretical principles that can be observed through simulations with Multisim software and measurement. Before using this document the board should be assembled, following the "ECG Simulator Assembly Instructions" procedures.

ECG Simulator Overview

Figure 1 shows a schematic diagram of the ECG Simulator kit. The circuit has a digital block, formed by two frequency dividers (integrated circuits IC1 and IC2) and the analog output network, which shapes the heart electrical signal. The switch S2 selects the cardiac rate, which can be either 1 Hz or 2 Hz (60 bpm/120 bpm).
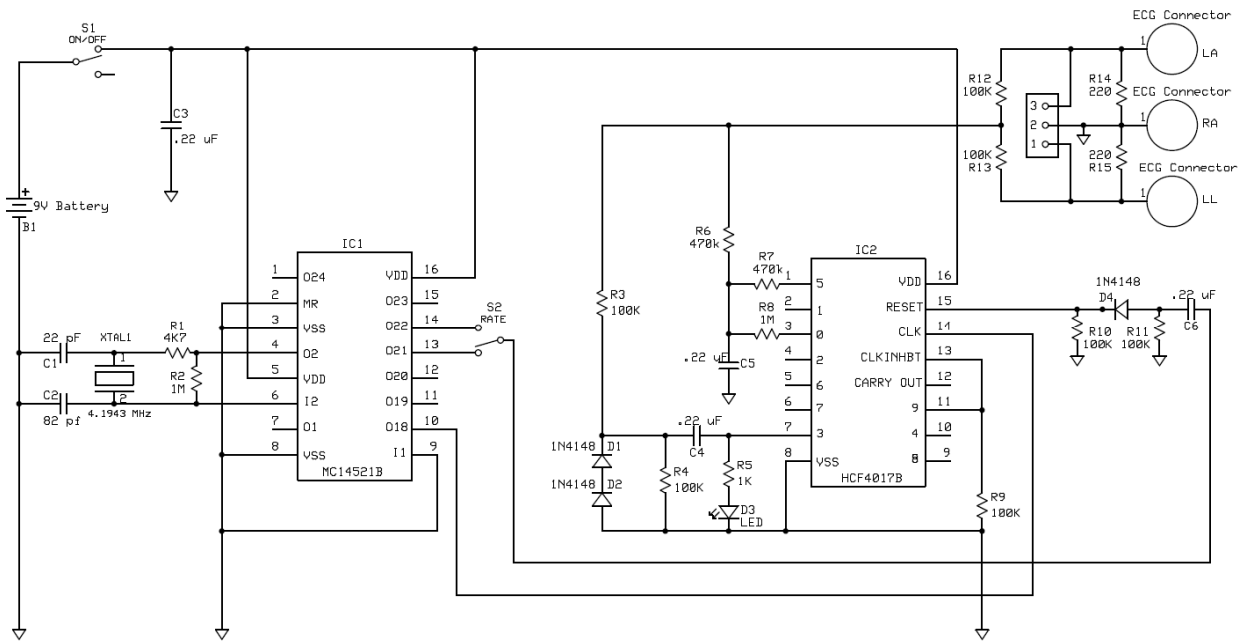

Figure 1 – ECG Simulator electronic schematic diagram.

Oscillator and Frequency Divider

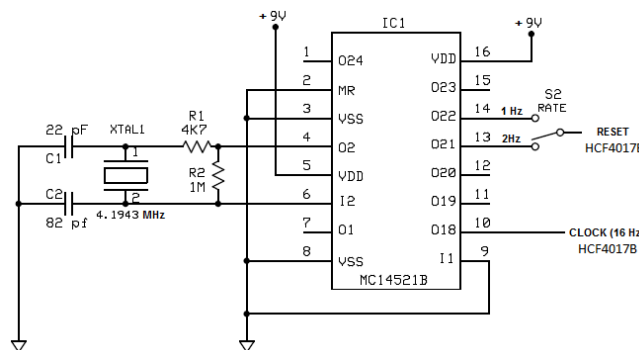The first digital block in Figure 2 corresponds to an oscillator and a 24 bits counter (IC1 - MC14521B).

Figure 2 – First frequency dividers stage formed by the MC14521B IC and the oscillator components.

This chip can generate its own clock in the inputs O2 and I2. The 4.1943 MHz crystal oscillating frequency is suggested by the manufacturer in datasheet[2] and can be used to generate sub-frequencies such as 1 Hz and 2 Hz.

The MC14521B is able to divide the frequency through a chain of 24 toggle (T) flip–flops. This kind of circuit can be built with a basic JK flip–flop logic, connecting the "J" and "K" inputs in the "T" node and keeping the voltage level in the high logic (9 V). In this case, the circuit will only change the output state "Q" when the clock signal "CP" rises, as shown in Figure 3.[3]
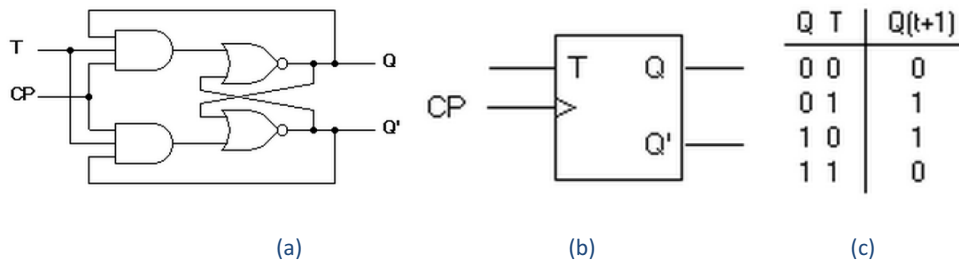

(a)　　　　　　　　(b)　　　　　　　　(c)

Figure 3 – Toggle flip-flop Logic diagram (a), graphical symbol (b) and transition table (c).[3]

Each block of the circuit above divides the input frequency by 2. Since the MC14521B has 24 T flip-flops, it is able to count until 2^{24} (16,777,216). After this value is reached, the circuit resets and restarts the counting. Due to the small number of pins available in the packaging, only outputs O18 until O24 are physically available, as seen in Figure 4.
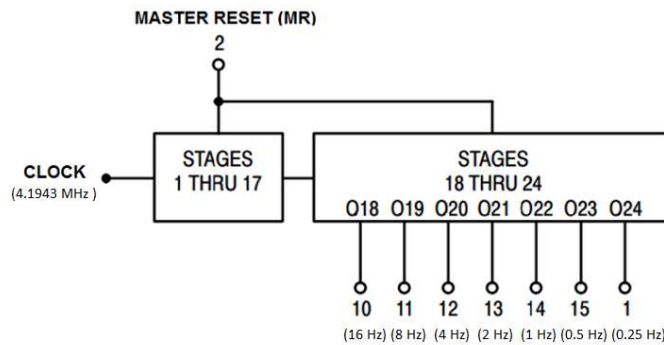

Figure 4 - MC14521B block diagram; the outputs of the last seven stages are available for additional flexibility.[2]

A 4.1943 MHz clock produces a 0.25 Hz signal in the last counter O24. This signal is much lower than a normal ECG signal; therefore, outputs of the earlier stages are used in this application, as shown in Table 1. The O18 signal is the clock (16 Hz) for the second integrated circuit IC2 (HCF4017B). The switch S2 selects the outputs O21 or O22 to reset this chip, changing the output rate either to 60 bpm or 120 bpm.

Table 1 - MC14521B output frequencies for a 4.1943 MHz input clock. O21 and O22 signals are used to select the heart rate, depending of the position from the S2 switch.

Output	Pin	Dividing factor	Frequency (Hz)	Period (s)
O18	10	2^{18} = 262 144	16	0.0625
O21	13	2^{21} = 2 097 152	2	0.5 (120 bpm)
O22	14	2^{22} = 4 194 304	1	1 (60 bpm)

Reset Circuit

Between both ICs there is a differentiator block (Figure 5), formed by C56 and R11. Although this circuit does not change the signal frequency, it converts the square wave input into an impulse signal that will be used later to reset the second stage (HCF4017B).
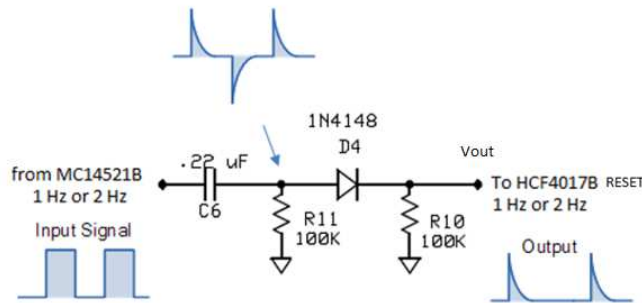

Figure 5 – Circuit that converts a square wave input signal into an impulse that is used to reset the following IC.

For the rising of the input signal, the diode D4 will conduct, and the differentiator output voltage (V_{out}) can be calculated by the Equation 1: [4]

$$V_{out} = (R_{11}//R_{10})C_6 \frac{dV_{in}}{dt} \tag{1}$$

Since the input signal corresponds to a square wave and the time constant ($\tau = C_6 . R_{11}//R_{10} = 0.011$ seconds) is much smaller than the inverse of the maximum input frequency (0.5 seconds), one can apply Equation 2, which calculates the charging voltage for a series RC circuit:

$$V_{out} = V_{in} e^{\frac{-t}{(R_{11}//R_{10})C_6}} \tag{2}$$

Figure 6 shows the output voltage of the differentiator block (blue) for a 9 V step signal in the input (red).
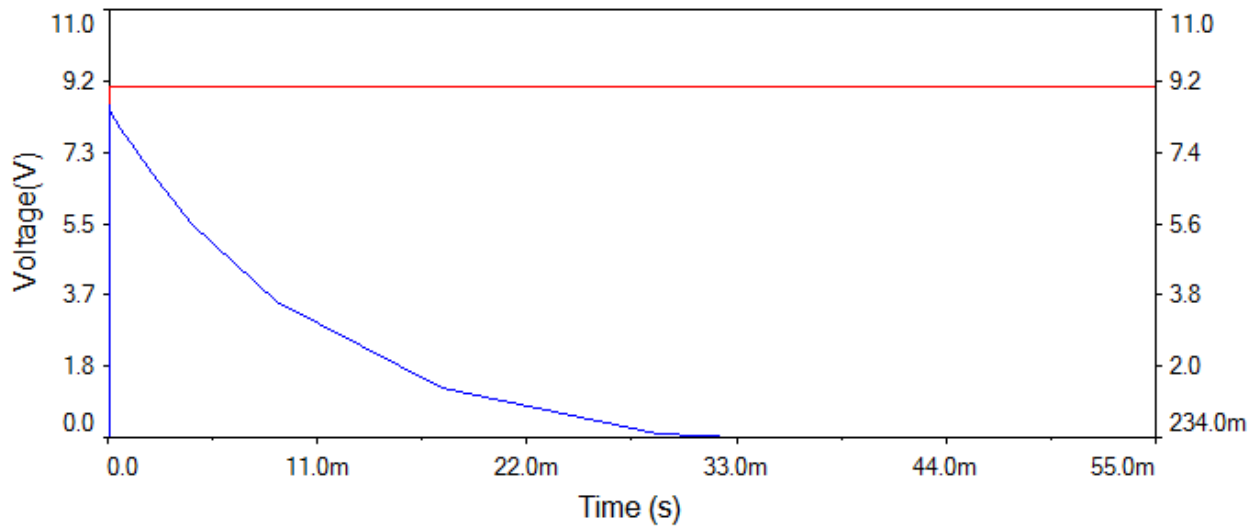
Figure 6 – Multisim simulation of the differentiator block input voltage (red) and the output curve (blue).

For this differentiator circuit, whenever the input signal drops from 9 V to 0 V, the diode D4 opens and the output voltage of the differentiator block remains 0 V. If there was no diode, this block would produce a negative impulse with similar shape as the blue curve in Figure 6. This signal could cause an undesired reset phase or even damage the next digital block.

Ring Counter

Although the IC2 (HCF4017B) in Figure 7 is also called a frequency divider, this component works as a Johnson counter with 10 decoded outputs that follow a ring counter pattern.[5]
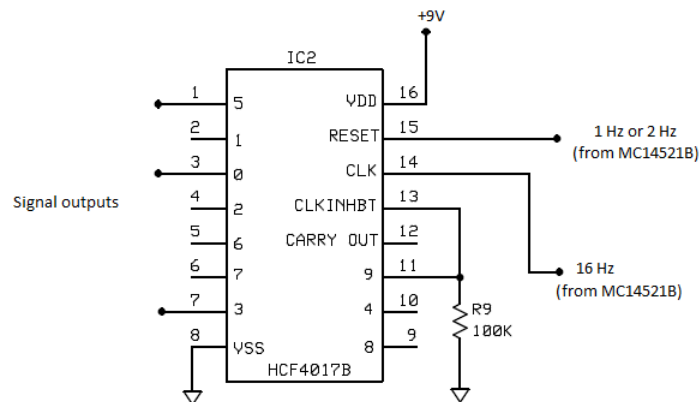

Figure 7 - Johnson Counter (HCF4017B) pins which are used to generate the Electrocardiogram wave.

The basic circuit that can be used to simulate the HCF4017B principle is Data (D) flip–flop. This kind of logic forwards the level in the D input whenever the clock signal CP rises, as shown in Figure 8.[3]

<div align="center">
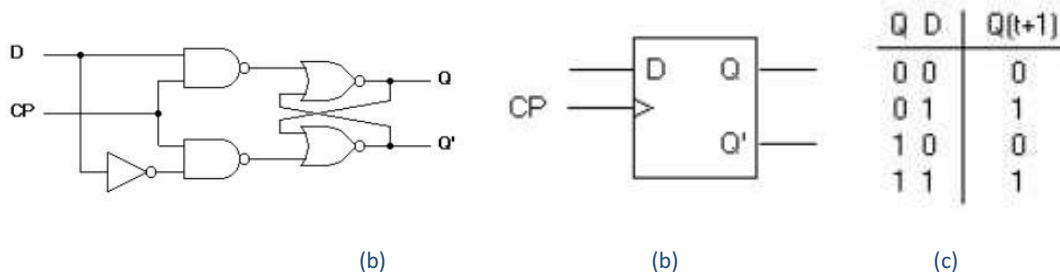
(b)   (b)   (c)

</div>

Figure 8 – Data flip-flop Logic diagram (a), graphical symbol (b) and transition table (c).

The HCF4017B outputs works in a similar patter as the chain of 10 Data (D) flip–flops in Figure 9. In this circuit, the value of each stage is shifted from left to right through each of the flip- flops, as shown in Figure 10. The duration of the high level (9 V) in all channel is twice the clock period (2*1/16 Hz = 0.125 seconds), however, each pin will be high in different time slots.
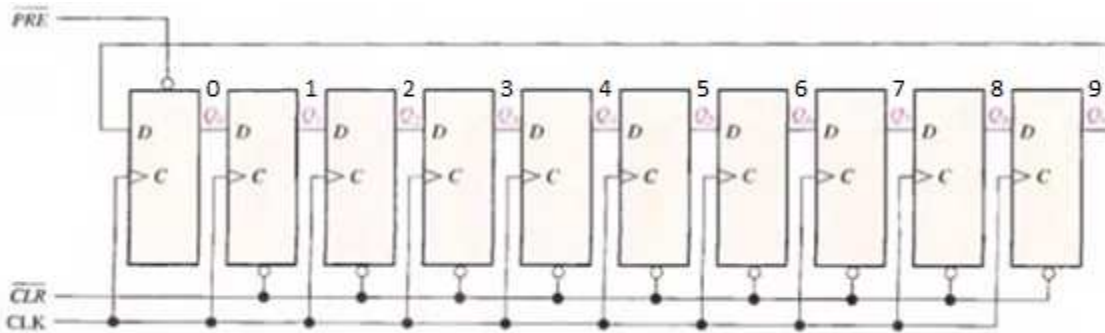

Figure 9 – 10 bits Ring counter block diagram; the circuit restarts the counting after the last bit is set to high logic.

Although there are 10 outputs available, only three (0, 3 and 5) are required to simulate the peaks components P, R and T of the ECG wave form, as seen in Figure 11. If the switch "S2" selects 120 bpm, which corresponds to a 2 Hz reset frequency, the HCF4017B will reset when the output "7" is in high logic level. However if this switch selects 60 bpm (1 Hz), the IC will restart to count after the 10th clock cycle, causing undesired signals in the output. This problem is solved connecting signal "9" to the "CLOCK INHIBIT" input, therefore freezing the outputs until the next reset signal, as seen in Figure 11.
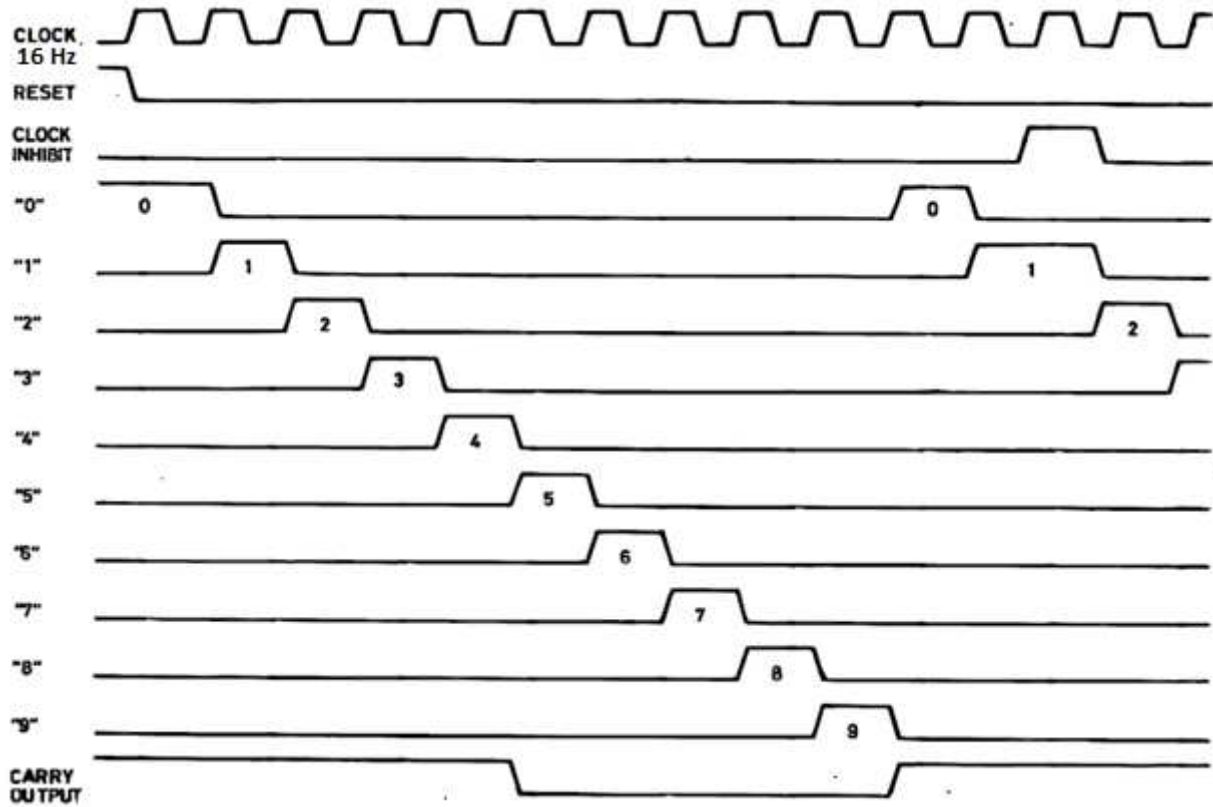
Figure 10 - Timing diagram of the HCF4017B counter output signals, each output will stay 0.125 seconds in high level (9 V).[5]

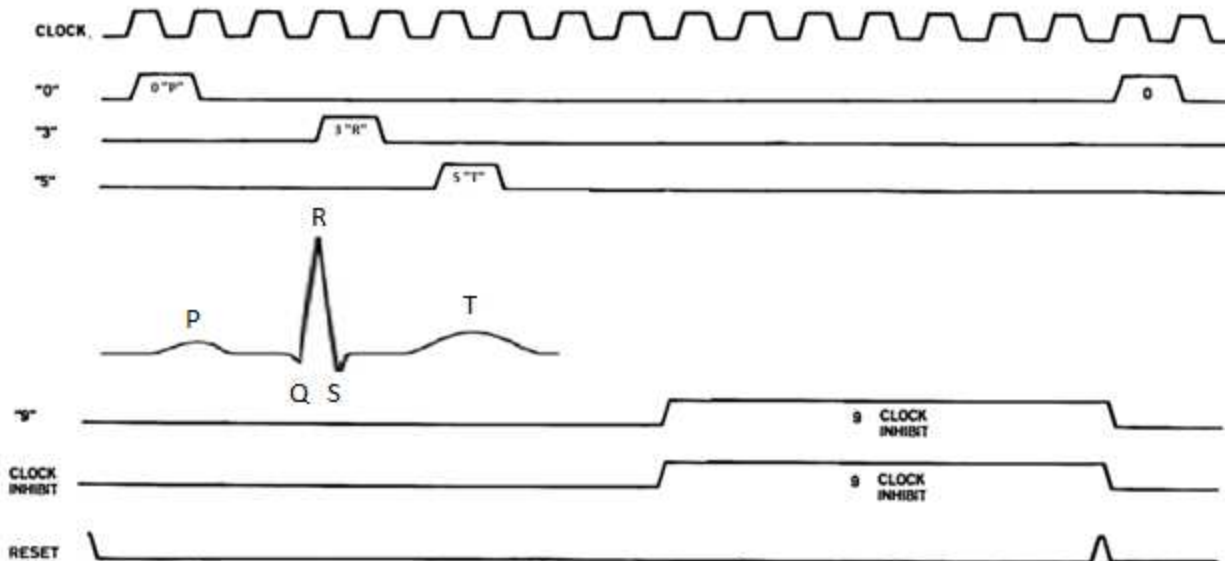Figure 11 – Outputs 0, 3 and 5 from HCF4017B compared with an ECG signal.

Output Signal Conditioning

The third stage in the simulator corresponds to a network of resistors that sums their current to shape the ECG wave. Since the HCF4017B has CMOS technology, whenever the logic level is zero, one can consider the outputs as open, which allow the analysis of each circuit branch separately. As already described in the earlier section, only the P, R, S and T sections are generated.

1. P Wave Circuit

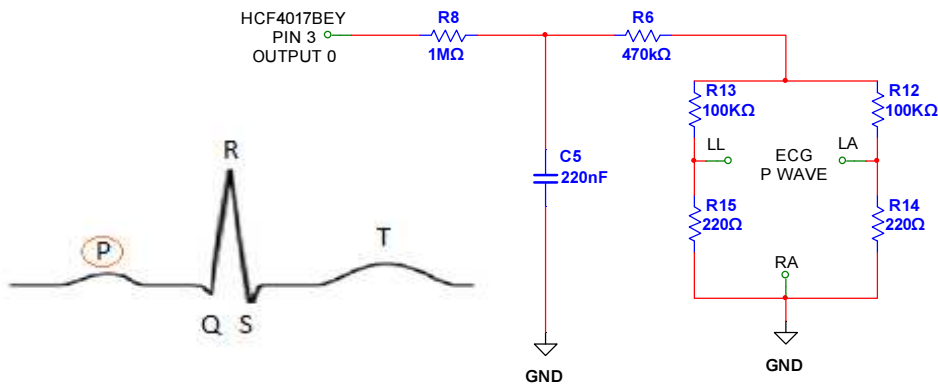Figure 12 shows the circuit responsible for the P wave

Figure 12 – P wave output circuit.

Since the resistor R13 is the same value as R12, and R15 is the same as R14, one can simplify the circuit, as shown in Figure 13. Whenever the logic level is "1", there is 9 V applied to the circuit, while in logic "0", the contact is open.
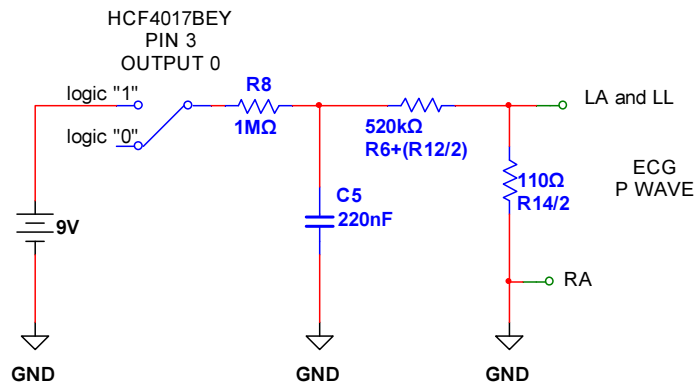

Figure 13 – Simplified circuit for P wave signal.

In order to calculate the signal in the outputs LL and LA, one needs first to analyze the voltage in the capacitor C5. The Thevenin's theorem[4] can be used during the capacitor charge, removing this component from the circuit and calculation E_{TH} and R_{TH} for the connections in Figure 14 in Equation 3 and 4.
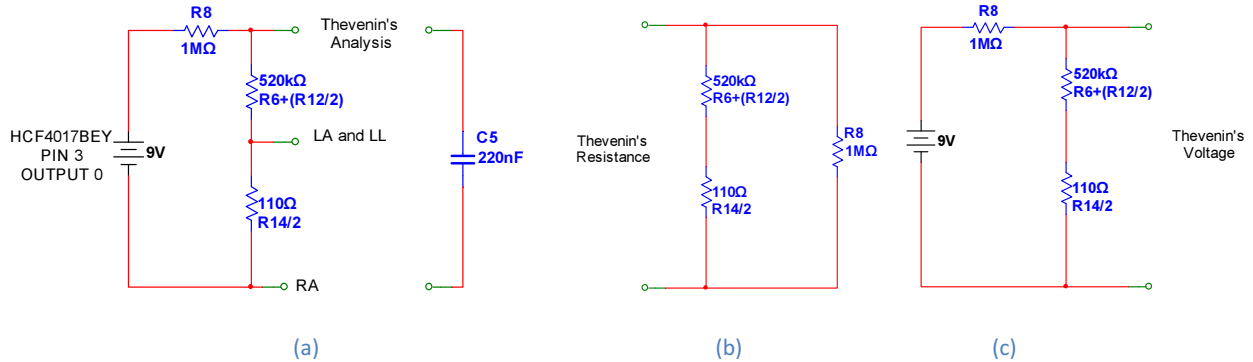

Figure 14 – Thevenin's theorem analysis of the P wave circuit during the logic "1". One needs to remove the capacitor C5 (a) and calculate the Thevenin's Resistance (b) and voltage (c).

$$R_{TH} = (520k + 110)//1M = 342.11 \ k\Omega \qquad (3)$$

$$E_{TH} = \frac{9}{1M + 520k + 110}(520k + 110) = 3.07 \ V \qquad (4)$$

Since the IC2 can be considered a step signal, one can approximate the charging voltage in the capacitor in Figure 15 though Equation 5.
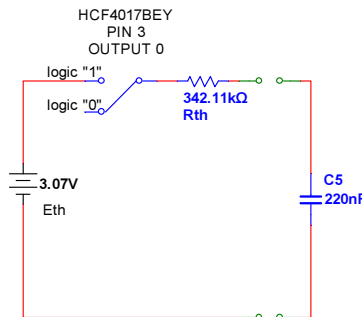

Figure 15 – Thevenin's analysis of C5 charging circuit for P wave signal.

$$VC5_{Charge} = 3.07(1 - e^{\frac{-t}{(342.11k*220n)}}) \qquad (5)$$

After finding the charging voltage in the capacitor C5, one can calculate the signal in the outputs LL and LA as seen in Figure 16 and Equation 6.
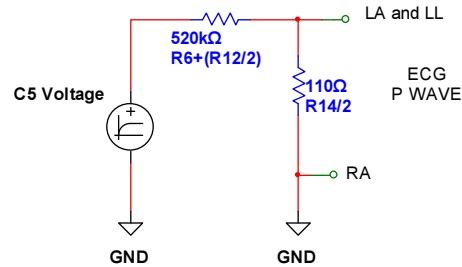
Figure 16 – P wave output circuit during the charge of the capacitor C5 (while pin 3 is in logic "1").

Equation 6 shows the how to calculate the P waveform output whenever the HCF4017B pin 3 is in logic "1".

$$VLA_{P\_logic1} = VLL_{P\_logic1} = \frac{3.07\left(1 - e^{\frac{-t}{(342.11k*220n)}}\right)}{520k + 110}(110) = 0.649m\left(1 - e^{\frac{-t}{(0.0753)}}\right) \qquad (6)$$

Although the maximum voltage in the capacitor C5 should be 3.07 V (Equation 5) and in the contacts LL and LA are 0.649 mV (Equation 6), the HCF4017B pin 3 will open before the capacitor charges completely, which corresponds to the instant 62.5 ms (1/16 Hz). Therefore, the resulting maximal voltages in C5 is 1.73 V (Equation 7) and in pins V_{LL} and V_{LA} is 0.366 mV (Equation 8).

$$VC5_{t=62.5ms} = 3.07\left(1 - e^{\frac{-0.0625}{(342.11k*220n)}}\right) = 1.73\,V \qquad (7)$$

$$VLA_{P\_t=62.5ms} = VLL_{P\_t=62.5ms} = \frac{1.73}{520k + 110}(110) = 0.366mV \qquad (8)$$

When the HCF4017B output 0 (pin 3) opens (logic "0"), the capacitor C5 will discharge with the circuit in Figure 17 through the Equation 9.
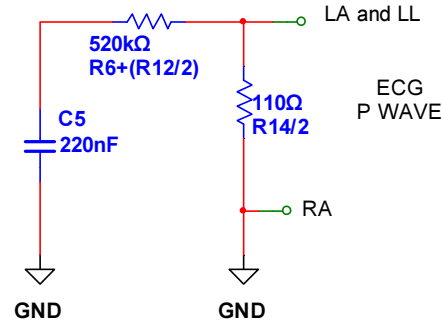
Figure 17 – P wave output circuit during the discharge of the capacitor C5 (while pin 3 is in logic "0").

$$VC5_{Discharge} = 1.73(1 - e^{\frac{-t}{(520.11k*220n)}}) \tag{9}$$

Equation 10 calculates the voltages in the pins VLA and VLL during the discharge of the capacitor C5 (logic "0").

$$VLA_{P\_logic0} = VLL_{P\_logic0} = \frac{1.73\left(1 - e^{\frac{-t}{(520.11k*220n)}}\right)}{520k + 110}(110) = 0.366m\left(1 - e^{\frac{-t}{(0.114)}}\right) \tag{10}$$

Figure 18 shows the signal created through this RC circuit to simulate the P waveform. Notice that the time constant is different for the rise and fall of the voltage, since the Thevenin's Resistance is smaller than the value in the discharge circuit.
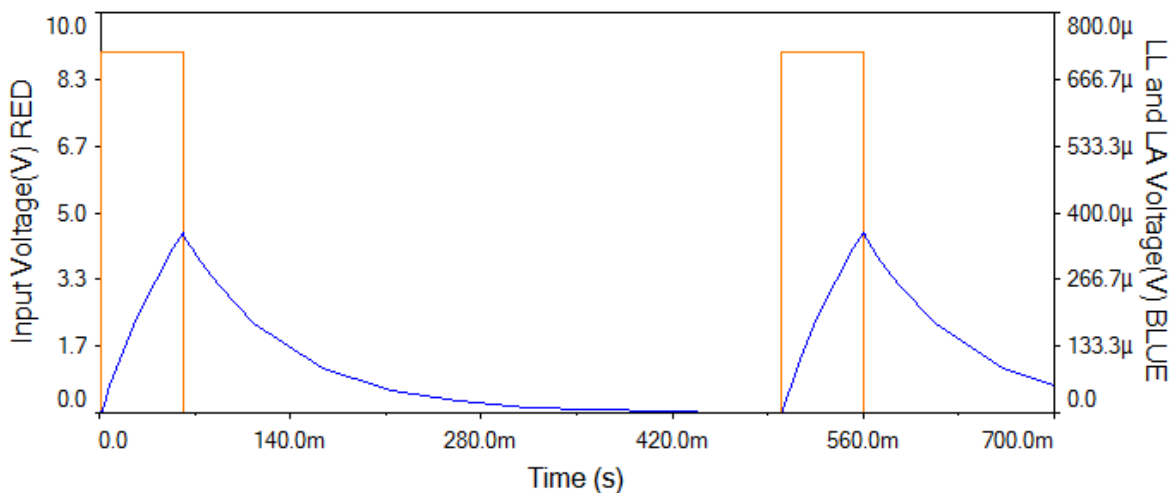

Figure 18 – Multisim simulation of the input square wave (red) and resulting P wave component (blue).

2. R and S Wave Circuit

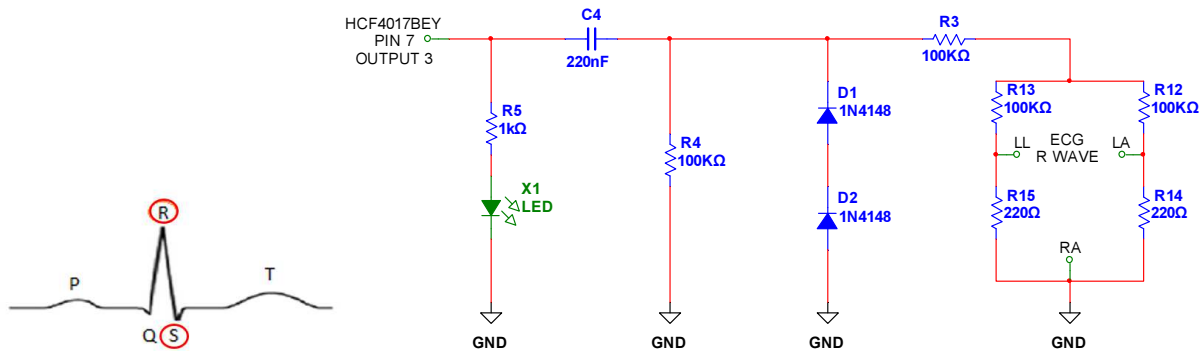Figure 19 shows the circuit that supplies the R and S wave segment.

Figure 19 – R, S wave output circuit.

The resistor R5 and the LED X1 are placed parallel to the output 3 to allow a visual control from the signal frequency and do not interfere in the R waveform. As in the reset circuit, the diodes D1 and D2 are used to avoid negative voltages. However, for a + 9 V step in the input, these parts are opened and can be disregarded. Therefore, one can simplify the R wave circuit as in Figure 20.
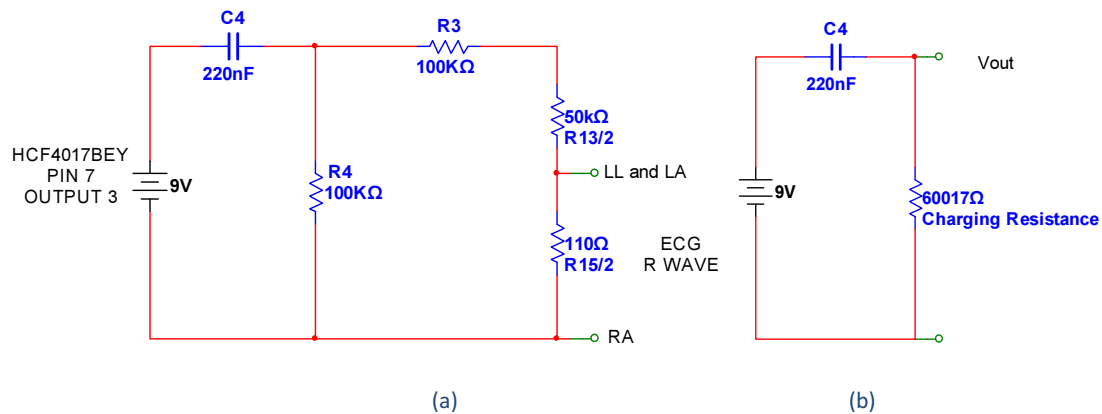

(a)   (b)

Figure 20 – Simplified circuit for R waveform (a) and equivalent resistance for the charge of the capacitor C4 (b).

Using the same principle of the differential circuit in the reset section, one can calculate the voltage in the equivalent resistor (V_{out}) through Equation 11. Equation 12 calculates the R signal curve, shaped when output 3 is in logic "1" (9 V). One can observe that the maximum voltage in contacts LL and LA is 6.57 mV, in the instant t= 0 seconds.

$$V_{out} = 9e^{\frac{-t}{(60017*220n)}} \tag{11}$$

$$VLA_R = VLL_R = \frac{\left(9e^{\frac{-t}{(60017*220n)}}\right)}{150110}(110) = 6.57m * e^{\frac{-t}{(60017*220n)}} \tag{12}$$

Figure 21 shows the equivalent circuit for the moment the output 3 (pin 7) from the HCF4017B opens. The configuration of two diodes in series (D1 + D2 = 1.2 V) was chosen to generate a small negative voltage, This voltage creates an S wave in the LL and LA pins, which can be calculated through the circuits in Figure 21.
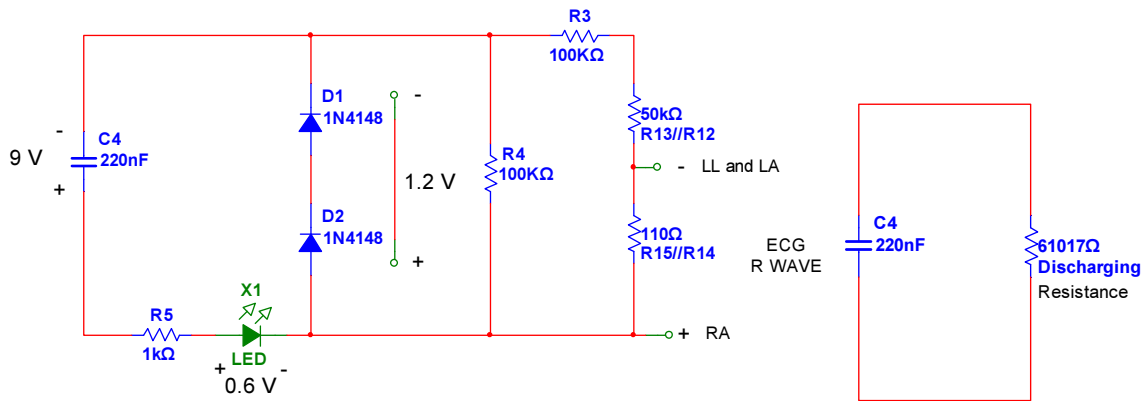

Figure 21 – S waveform circuit (a) and equivalent discharge resistance for the capacitor C4 (b).

However, in this case, an initial voltage of - 1.2 V is limited by D1 and D2 series, as seen in Equation 13.

$$VLA_S = VLL_S = \frac{\left(-1.2e^{\frac{-t}{(61017*220n)}}\right)}{150110}(110) = -0.88m * e^{\frac{-t}{(61017*220n)}} \tag{13}$$

Figure 22 shows the simulated wave for the R and S circuits.
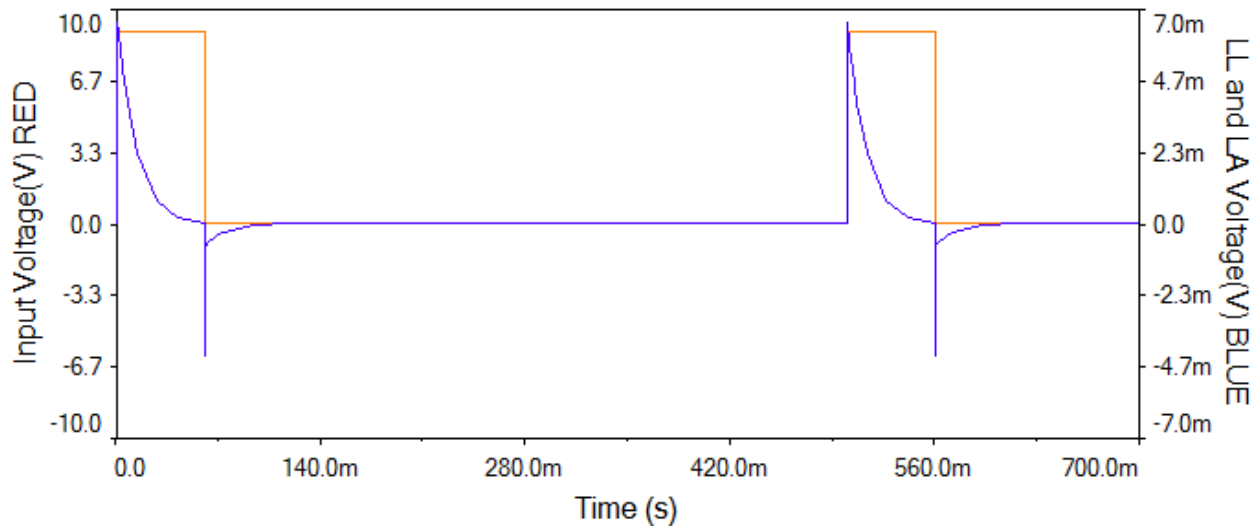
Figure 22 – Multisim simulation of the input square wave (red) and resulting R and S waves component (blue).

3. T Wave Circuit

The last component of the ECG signal is the T wave. The circuit that shapes this signal (Figure 23) is almost the same as the P wave, except that in pin 1, the series resistance value decreases from 1 MΩ to 470 kΩ. This will also decrease the charging time and therefore, the amplitude of the T signal should be higher than the P component.
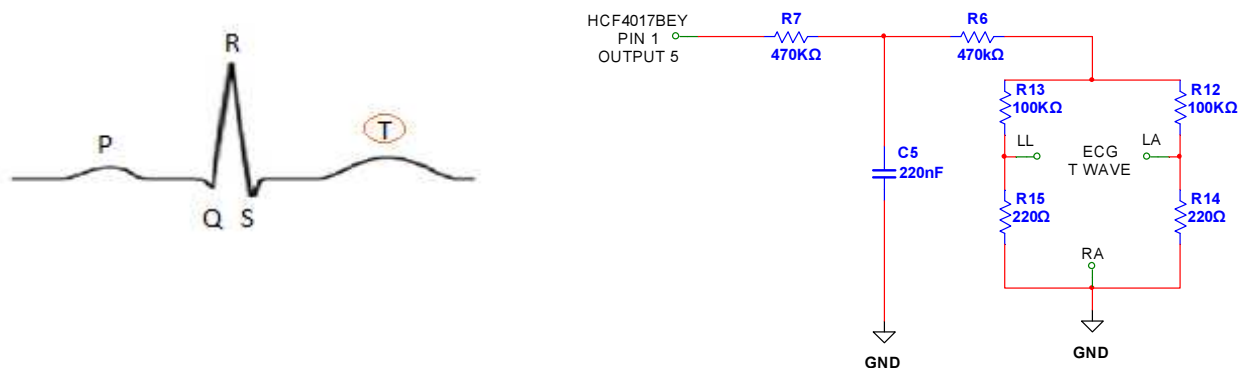
Figure 23 – T wave output circuit.

In this case one can repeat Thevenin's theorem (Figure 24) and also use a step signal to calculate the voltage in the capacitor through the charge Equation 14.
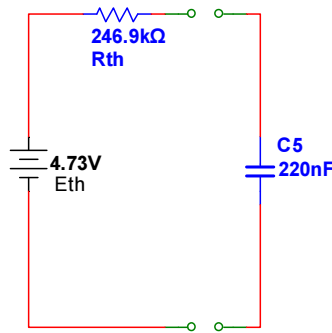
Figure 24 – C5 charging circuit for Thevenin's analysis of the T wave circuit.

$$VC5_{Charge} = 4.73(1 - e^{\frac{-t}{(246.9k*220n)}}) \tag{14}$$

After finding the charging voltage in the capacitor C5, one can calculate the signal in the outputs LL and LA as seen in Figure 16 (P and T wave have the same capacitor discharge circuit) and Equation 15.

$$VLA_{T\_logic1} = VLL_{T\_logic1} = \frac{4.73(1 - e^{\frac{-t}{(246.9k*220n)}})}{520k + 110}(110) = 1m\left(1 - e^{\frac{-t}{(0.054)}}\right) \tag{15}$$

Although Equation 14 and Equation 15 shows that the maximum voltage in the capacitor C5 is 4.73 V and in the contacts LL and LA is 1 mV, the input signal will drop to zero before the capacitor charges completely, which corresponds to the instant 62.5 ms (1/16 Hz). If one replaces this value in Equations 14 and 15, the maximum capacitor charge is 3.23 V and the T wave voltages V_{LL} and V_{LA} are both 0.68 mV. Equation 16 shows the voltage during the discharge of the capacitor C5 for the T wave segment.

$$VC5_{Discharge} = 3.23(1 - e^{\frac{-t}{(520.11k*220n)}}) \tag{16}$$

The T wave discharge circuit is the same for the P wave (Figure 17). Therefore the ECG simulator output in the logic "0" can be calculated through the Equation 17.

$$VLA_{T\_logic0} = VLL_{T\_logic0} = \frac{3.23(1 - e^{\frac{-t}{(520.11k*220n)}})}{520k + 110}(110) = 0.68\ m\left(1 - e^{\frac{-t}{(0.054)}}\right) \quad (17)$$

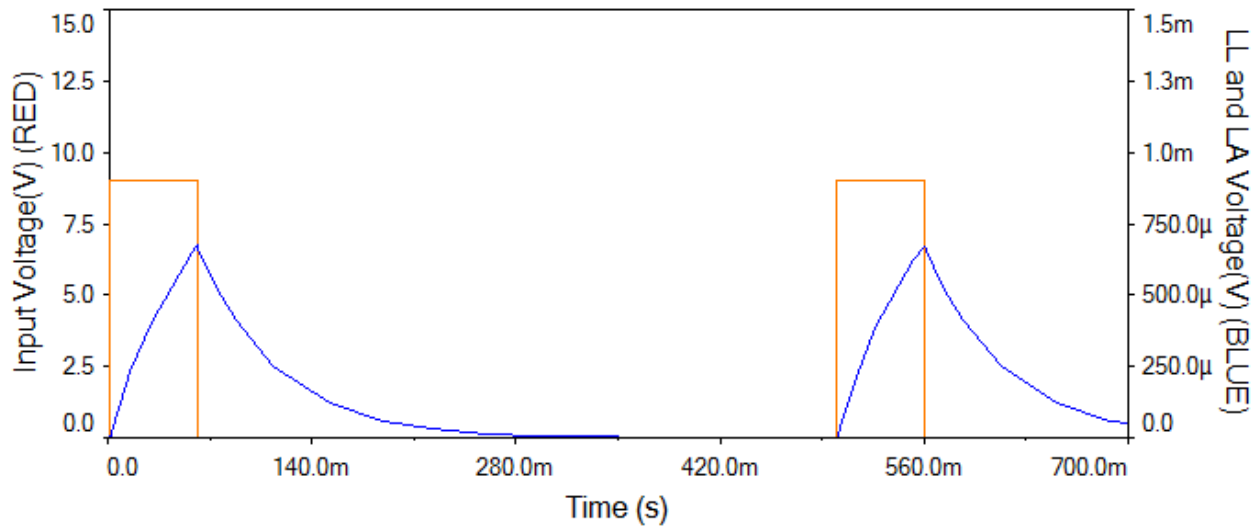Figure 25 shows the simulated wave for the T circuit.

Figure 25 – Multisim simulation of the input square wave (red) and resulting T wave component (blue).

4. Final Waveform

The simulation of the final waveform can be created by adding each circuit output, as shown in Figure 26. The red curve corresponds to the P part; the blue represents the R and S peaks, and the green shows the T segment. If the rate selection switch is in the 120 rpm position, the signal will start to raise again after 0.56 seconds. If this switch is set to 60 rpm, the signal will remain in 0 V until 1.05 seconds and then restart the P peak.
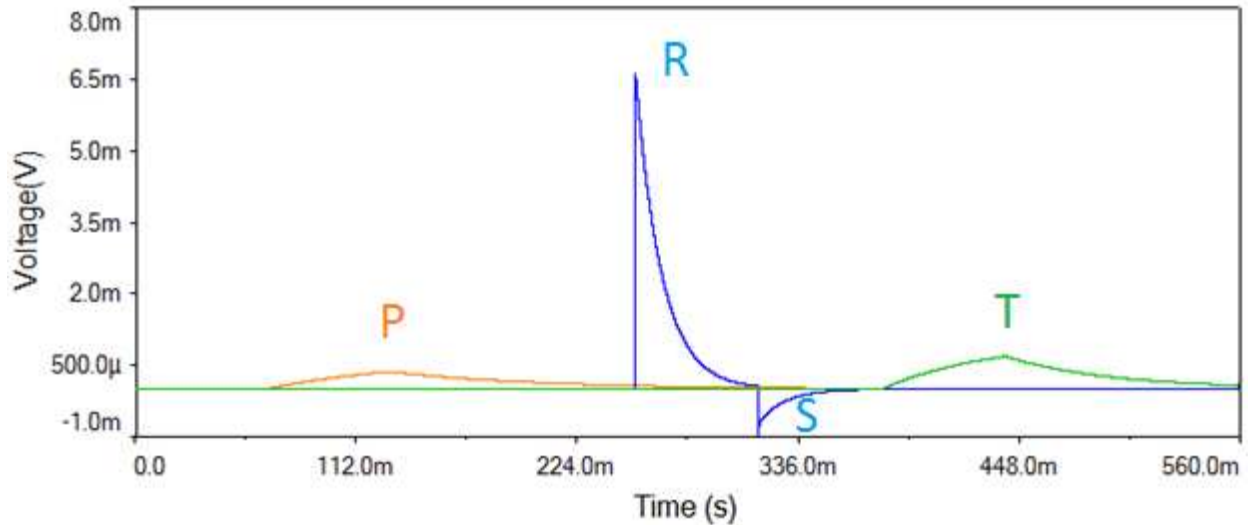
Figure 26 – Multisim simulation of the of the final ECG signal. The red curve corresponds to the P part; the blue represents the R and S peaks, and the green shows the T segment.

References

1. Webster, J. G. *Medical Instrumentation Application and Design [Hardcover]*. 720 (Wiley; 4 edition, 2009).

2. ON Semiconductors. MC14521B, 24 - Stage Frequency Divider. (2013). at <http://www.onsemi.com/pub_link/Collateral/MC14521B-D.PDF>

3. Mano, M. M. *Digital design*. 492 (Prentice-Hall, 1984).

4. Dorf, R. C. & Svoboda, J. A. *Introduction to Electric Circuits*. 886 (John Wiley & Sons, 2010).

5. STMicroelectronics. HCF4017B - Decade counter with 10 decoded outputs. (2001). at <http://www.st.com/st-web-ui/static/active/en/resource/technical/document/datasheet/CD00000366.pdf>

Appendix

1. Basic Heart Anatomy

The cardiovascular system is responsible for circulating blood throughout the body to supply the tissues with oxygen and nutrients. The heart is the muscle responsible for pumping blood to and through the vessels. It is divided into four chambers: right atrium, right ventricle, left atrium, and left ventricle, as seen in Figure 27. There are valves between each atrium and ventricle and in the ventricle output to prevent backward flow. The average adult cardiac rate is 60 beats per minute; however, this rate increases to 120 in the case of infants. The heart contraction stimulus is caused by an electrical signal that initiates at the Sinoatrial (SA) node, located at the top of the right atrium.
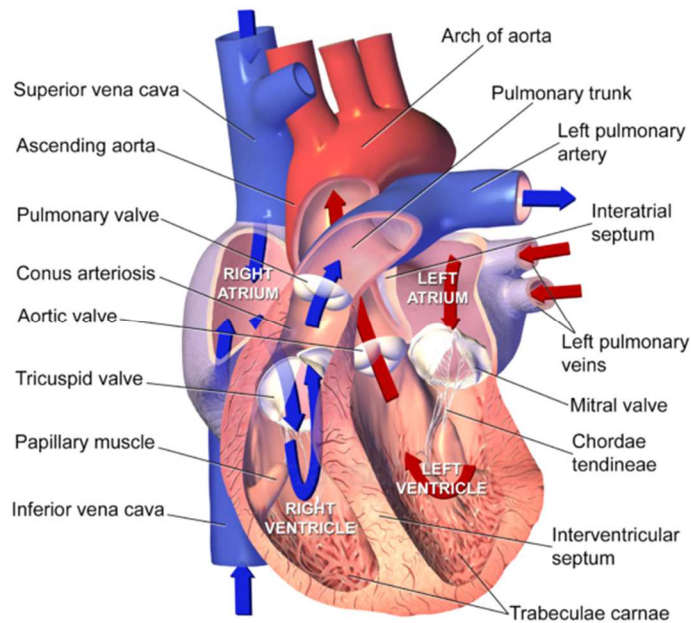

Figure 27 – Sectional anatomy of the heart (Blausen Medical Communications via Wikimedia Commons)..

2. Principles of Electrocardiography

The small electrical signal (mV) produced in the heart can be measured through a device called an electrocardiogram (ECG). This instrument allows the physician to know the rate and regularity of heartbeats, as well as the size and position of the chambers, the presence of any damage to the heart, and the effects of cardiac drugs or devices. A basic ECG requires at least three connections, which form the Einthoven's triangle in Figure 28.
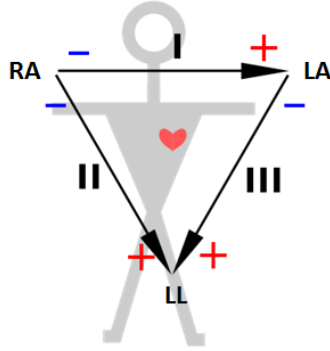
Figure 28 – Einthoven's triangle. Signal I corresponds to the traditional ECG waveform (Kychot via Wikimedia Commons).

Signal I shows the voltage between the (positive) left arm (LA) electrode and the right arm (RA) electrode:

$$I = LA - RA$$

Signal II shows the voltage between the (positive) left leg (LL) electrode and the right arm (RA) electrode:

$$II = LL - RA$$

Signal III shows the voltage between the (positive) left leg (LL) electrode and the left arm (LA) electrode:

$$III = LL - LA$$

The electronic component used for ECG measurement is called an instrumentation amplifier. It has a high gain (multiplies many times the original signal) and requires very low input currents. Inside of this amplifier, there are differential blocks, such as in Figure 29. These circuits are able to measure signals I, II and III directly from the patient's leads.
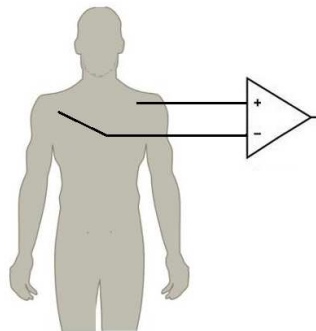

Figure 29 – The ECG measurement circuit uses a differential amplifier to subtract the voltages between the right and left arm (BotMultichill via Wikimedia Commons).

Figure 30 shows a standard ECG signal (II) divided into five parts: P-QRS-T. The P wave represents atrial depolarization, and the QRS represents ventricular depolarization. The T wave reflects the phase of rapid repolarization of the ventricles.
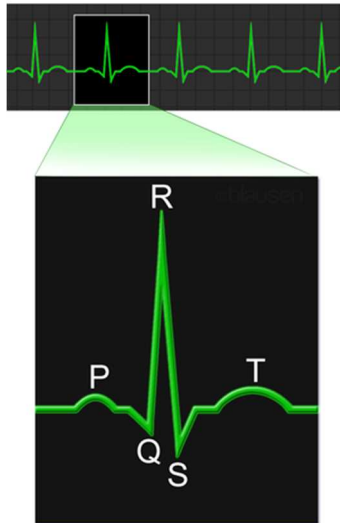

Figure 30 – Normal heart beat electrocardiogram wave signal (Blausen Medical Communications via Wikimedia Commons).

3. Parts List

The EWH ECG Simulator package should contain the Printed Circuit Board (PCB) and the components listed in Table 2. Do not remove them from the package until you read the "Assembling Instructions" document. **Error! Reference source not found.** If mixed, some parts cannot be identified without test instruments.

Table 2 – ECG Simulator Kit part list.

Description	Value	Quantity	Schematic ID
Resistor	4700 Ohm (4K7)	1	R1
Resistor	1,000,000 Ohm (1M)	2	R2, R8
Resistor	100, 000 Ohm (100K)	7	R3, R4, R9, R10, R11, R12, R13
Resistor	1,000 Ohm (1K)	1	R5
Resistor	470,000 Ohm (470K)	2	R6, R7
Resistor	220 Ohms	2	R14, R15
Capacitor	22 Pico farad (22 pf)	1	C1
Capacitor	82 Pico farad (82 pf)	1	C2
Capacitor	220 Nano farad	4	C3, C4, C5, C6

	(.22 uf)		
Diode	1N4148	3	D1, D2, D4
LED	3 mm red	1	D3
Integrated Circuit	4521	1	IC1
Integrated Circuit	4017	1	IC2
Crystal	4.1943 MHz	1	XTAL1
ECG Connectors Sew-on Snaps	N/A	3	ECG Connectors (LA, RA, LL)
ECG Connector Header Contact	N/A	1	N/A
Switches	N/A	2	S1, S2
Battery Connector	N/A	1	N/A
PCB Rubber Feet	N/A	4	N/A
Printed Circuit Board	N/A	1	N/A